Sub A17

ABSTRACT

CHIP SCALE PACKAGE WITH FLIP CHIP INTERCONNECT

A flip chip package is formed by a solid-state bond technique for connecting the input/output pads on the integrated circuit chip and the package substrate. The solid-state bond technique involves a direct mating of metal surfaces, and does not employ any particulate conductive material. Accordingly the connections are capable of carrying very high current, and display good long-term reliability as compared to ACA or ICA particulate interconnects. Moreover the solid-state bond technique does not entail a melting or flow of any interconnecting material. Accordingly the connections can be formed at very fine geometries, typically as low as 70 micrometers pitch. Also, the space between the surface of the integrated circuit chip and the subjacent surface of the package substrate is filled with a patterned adhesive structure, which consists of one or more adhesive materials that are deployed in a specified pattern in relation to the positions of the second level interconnections between the package and the printed circuit board. According to this aspect of the invention, the coefficient of thermal expansion and the compliancy of the package structure in the regions overlying the second level connections can be tailored to reduce potentially damaging propagation of stress generated in the second level connections on the package to features on the integrated circuit chip, and thereby extending the long-term reliability of the package and of the interconnects.